REMARKS

Claims 1-16 are pending. Claims 2, 3, 4, 7, 13 and 14 have been amended; claims 1-4, 6 and 7 are independent. Reconsideration in view of the following remarks is kindly requested.

I. ENTRY OF AMENDMENT AFTER FINAL

Applicants request entry of this Amendment after Final in that all amendments made herein have been made merely to overcome the objections raised by the Examiner, and/or to rewrite dependent claims in independent form. These amendments do not raise any new issues requiring further consideration and/or search.

II. CLAIM OBJECTIONS

Applicants have amended claims 13 and 14 taking into account the suggestions and comments made by the Examiner. Therefore, withdrawal of this objection is kindly requested.

III. REJECTION UNDER 35 U.S.C. § 103

The Examiner rejects claims 1, 4-6 and 12 under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicants' Admitted Prior Art ("AAPA"), U.S. Patent Publication No. 2002/0140661 ("Miyajima"), and U.S. Patent No. 5,615,376 ("Ranganathan"). This rejection is respectfully traversed.

A. THE COMBINATION OF RANGANATHAN WITH AAPA AND/OR MIYAJIMA WOULD RENDER THE SYSTEM OF AAPA AND/OR MIYAJIMA INOPERATIVE.

The rejection should be withdrawn because combining Ranganathan with AAPA and/or Miyajima would render the systems of AAPA and/or

Miyajima inoperative. The Examiner correctly recognizes that both AAPA and Miyajima fail to teach a driving control circuit, "stopping driving of the clock signal generation circuit in the inaction period," as set forth in claim 1.[1] As in the previous Office Action, the Examiner relies upon Ranganathan to allegedly teach this feature.

In support of the alleged combination, the Examiner states that the skilled artisan would be motivated to combine the teachings of Ranganathan with AAPA and Miyajima in order to, "create a method for conserving power by managing the various clocks and to disable them when they are not needed."[2] Applicants disagree in that the skilled artisan would clearly **not** have been motivated to combine the teachings of AAPA, Miyajima and/or Ranganathan to arrive at the claimed invention as claimed in claim 1, for example.

In the display device of AAPA, the clock signal generation circuit 106 of Fig. 12 **must operate during the non-scanning period** (i.e., the inaction or non-scanning period) so as to supply a dot clock to the H counter 107 and the V counter 108. The display device of AAPA could not be modified with the teachings of Ranganathan such that the driving of the clock signal generation circuit is stopped **because** as a result of the modification, **the display device of AAPA would cease to operate as intended and be rendered inoperative.**[3] Therefore, the skilled artisan would not have combined AAPA with Ranganathan at the time the invention was made.

---

[1] Office Action, pp. 5.
[2] Office Action, pp. 5.
[3] See, specification, page 22, first full paragraph.

Furthermore, the Examiner relies upon the timing control 160 of Miyajima as allegedly teaching the "clock signal generation circuit for generating a clock signal," as set forth in claim 1, for example.[4] However, similar to that discussed above with regard to AAPA, modifying Miyajima with the teachings of Ranganathan such that the driving of the timing control 160 is stopped renders the system of Miyajima inoperative.

As shown in Fig. 5 of Miyajima, an enable signal ENA having a predetermined duration is output to the V driver 210 and the H driver 220 to stop output of gate signals by the V driver 210 and data line selection signals by the H driver 220. A timing control 160 predetermines the duration of the enable signal ENA based upon a master clock MCLK input to the timing control 160. That is, the timing control 160 of Miyajima is driven by the master clock MCLK.

As the Examiner should appreciate, the master clock signal MCLK cannot be interrupted or stopped because the timing control 160 would no longer have any reference for determining how long the output of the gate signals and the data line selection signals have been stopped (i.e., the length of the inaction period). That is, the timing control 160 **must receive the master clock signal MCLK at all times**. Therefore, Miyajima could clearly not be modified with the teachings of Ranganathan, **because** as a result of this modification **the system of Miyajima would cease to operate as intended and be rendered inoperative**.

---

[4] Office Action, pp. 5.

For at least these reasons, the skilled artisan would not have combined the teachings of Ranganathan with Miyajima and/or AAPA at the time the invention was made. As such, a *prima facie* case of obviousness has not been properly established and the Examiner's rejection under 35 U.S.C. §103(a) is clearly deficient.

The Examiner's rejection of claim 6 is also deficient for reasons somewhat similar to those set forth with regard to claim 1. Claims 2, 4 and 5 are dependent from claim 1 and thus the Examiner's rejection is deficient with regard to these claims as well. Withdrawal of the above rejection is requested.

IV. FURTHER REJECTIONS UNDER 35 U.S.C. § 103(a)

The Examiner further rejects claims 2 and 7 under 35 U.S.C. §103(a) as being unpatentable over AAPA, Miyajima, Ranganathan and U.S. Patent No. 6,088,806 ("Chee"); and claims 3, 8-11 and 13-16 under 35 U.S.C. §103(a) as being unpatentable over AAPA, Miyajima, Ranganathan, Chee and U.S. Patent Publication No. 2002/0180673 ("Tsuda"). This rejection is respectfully traversed.

A. THE DISPLAY DEVICES OF CLAIMS 2, 3, 7-11 AND 13-16 ARE NOT OBVIOUS OVER AAPA, MIYAJIMA, RANGANATHAN, CHEE AND/OR TSUDA.

Initially, the above rejections should be withdrawn because the Examiner's alleged combination of AAPA, Miyajima, Ranganathan, Chee and/or Tsuda is deficient for at least reasons somewhat similar to those previously set forth above.

Furthermore, the above rejection should be withdrawn because the display device of claim 3, for example, is not obvious over AAPA, Miyajima, Ranganathan, Chee and/or Tsuda. The display device of claim 3, for example, includes at least: (i) a clock signal (the fastest signal) generated by a clock signal generation circuit and used for taking a data signal into a data signal line; (ii) an output timing clock (e.g., a horizontal synchronization series signal); (iii) a start timing clock (e.g., a vertical synchronization series signal); and (iv) a control clock signal (e.g., a driving control signal). Each of these signals is different at least with respect to speed.

Moreover, one of the output timing clock, the start timing clock and the control clock signal is generated based on a base signal. The base signal is selected from another one of the output timing clock, the start timing clock and the control clock signal. In an inaction period defined by the control clock signal, the driving circuits and at least the clock signal are stopped, while the base signal is not stopped. This enables the display device of claim 3, for example, to carry out smooth scanning even if the scanning period and the inaction period are switched alternately. In addition, the display device of claim 3, for example, may save power by stopping at least one of the clocks including the clock signal.

To the contrary, however, none of AAPA, Miyajima, Ranganathan, Chee and/or Tsuda taken singly or in combination teach or suggest generating at least one of output timing clock, the start timing clock and the control clock signal (each of which are different in speed) based on one of the output timing

clock, the start timing clock and the control clock signal, but not the clock signal. Therefore, the display device of claim 3, for example, is not obvious over AAPA, Miyajima, Ranganathan, Chee and/or Tsuda taken singly or in combination. Withdrawal of the above rejection is requested.

V. CONCLUSION

In view of above remarks, reconsideration of the outstanding rejection and allowance of the pending claims is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Andrew M. Waxman, Reg. No. 56,007, at the number of the undersigned listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, PLC

By _____ 45,274

Donald J. Daley
Reg. No. 34,313

DJD/MJL/AMW:jcp

P.O. Box 8910
Reston, VA 20195
(703) 668-8000